Docket No.: 050006-0128 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Makoto NAGATA, et al.	:	Confirmation Number: 4496
Application No.: 09/977,994	:	Tech Center Art Unit: 2857
Filed: October 17, 2001	:	Examiner: Jeffrey R. West

For: METHOD AND APPARATUS FOR ANALYZING A SOURCE CURRENT WAVEFORM IN A SEMICONDUCTOR INTEGRATED CIRCUIT

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed February 16, 2005. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: May 16, 2005

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APPEAL BRIEF

Mail Stop Appeal Brief
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P.O. Box 1450
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed February 16, 2005, wherein Appellant appeals from the final rejection of claims 1-14.

Real Party In Interest

This application is assigned to Semiconductor Technology Academic Research Center by assignment recorded on October 10, 2001, at Reel 012277, Frame 0166.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1-14 are pending of which claims 1 and 7 are independent. Claims 1-14 stand rejected.

Status of Amendments

No amendment has been filed subsequent to the issuance of the Final Action dated November 16, 2004.

Summary of Claimed Subject Matter

As electronic devices in large-scale integrated ("LSI") circuits have been reduced in size, there has been increased generation of noise resulting from a change in source current flowing across the LSI circuit during operation, digital circuits that leak and dissipate via the silicon substrate, the LSI chip package, and the wirings on a printed circuit board.

Conventional methods that analyze the source current include (1) expanding the digital circuit to transistor level and using a circuit simulator to conduct a transition analysis from the waveform of the source current, and (2) approximating the waveform of consumed current at each logic gate, and summing the waveforms to generate an approximation of the source current. Disadvantageously, the first method requires extensive execution time and is unsuited for design optimization where the simulation has to be continually repeated. The second method suffers from poor accuracy, and is especially unsuited for analyzing noises that are sensitive to a change with time in the source current.

The claimed concepts overcome these problems and provide a novel method and apparatus of analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having multiple logic gates. The claimed features include representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit. Specifically, the digital circuit is represented as a time-division group of parasitic capacitors each connected between a source line and a ground line. Each parasitic capacitor of the time-division group of parasitic capacitors is to be charged at a specific timing. The representation further includes a group of parasitic capacitors each charged statically. Fig. 1 provides an exemplary illustration of such a digital

circuit representation including a time-division group of parasitic capacitors, designated by $\sum C_{ch,\uparrow}$ and $\sum C_{ch,\downarrow}$, and a group of parasitic capacitors to be charged statically, designated by $\sum C_{st}$ and C_s.

An analysis model is generated by (1) coupling one end of the time-division group of parasitic capacitors, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and (2) connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line. Accordingly, the waveform of the source current may be determined based on the analysis model. Fig. 2 provides an exemplary illustration in which the time-division group of parasitic capacitors are switched or connected in the time-division manner. In other words, each parasitic capacitor $C_{ch,\uparrow}$, $C_{ch,\downarrow}$, is charged or discharged at a certain interval of time T, forming a time-division group of parasitic capacitors.

Issues

Whether claims 1-6 and 8-14 stand properly rejected under 35 U.S.C. §103(a) as being unpatentable over Nagata et al., "Measurements and Analysis of Substrate Noise Waveform in Mixed Signal IC Environment" (hereinafter "Nagata") in view of U.S. Patent Application Publication No. 2002/0022951 to Heijningen et al. (hereinafter "Heijningen").

Whether claim 7 stands properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagata in view of Heijningen and further in view of Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in Wright" (hereinafter "Mitra").

Grouping of Claims

All claims are grouped together with claim 1.

Argument

I. Rejection of Claims 1-6 and 8-12 under 35 U.S.C. §103(a) – Nagata in view of Heijningen

Claim 1 reads as follows:

> A method of analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, comprising:
>
> representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit, as a time-division group of parasitic capacitors comprising parasitic capacitors each connected between a source line and a ground line to be charged at a specific timing, and a group of parasitic capacitors each charged statically;
>
> generating an analysis model by coupling one end of the time-division group of parasitic capacitors, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line; and
>
> determining the waveform of the source current in the digital circuit from the analysis model.

Nagata discloses a substrate noise analysis model for a mixed integrated circuit (IC) environment. Fig. 7 illustrates equivalent circuits of logic elements in which the switching action, defined in accordance with a truth table, charges or discharges load capacitance. A state of a group of logic circuits L is selected from a truth table for input N, which is applied to only the first logic gate L (See Nagata at Figs. 7b and 7c). Changing inputs to the first logic gate L affects other logic gates in this series, as outputs of each logic gate L are connected to inputs of subsequent logic gates in the series.

For any combination of inputs N selected, Nagata fails to identify which logic gates, if any, in the series will be activated or charged. The truth table of Nagata defines charging/discharging the parasitic capacitors at a certain instant. Nagata fails to disclose "representing the digital circuit,

according to a distribution of switching operations of the logic gates in the digital circuit, as a time-division group of parasitic capacitors," as claim 1 recites.

It follows that Nagata fails to disclose "generating an analysis model by coupling one end of the time-division group of parasitic capacitors, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line," as claim 1 recites. In fact, the truth table of Nagata dictates the manner in which connections are made and, as such, the group of parasitic capacitors are not "time-division." In other words, there is no division of time in which each of the parasitic capacitors is connected to a source and ground line (compare with Fig. 2).

Both the Appellant and the Examiner appear to agree that Nagata does not disclose or suggest the "time-division group of parasitic capacitors" and the waveform of the source current being determined based on the analysis model, as claim 1 recites. (Final Action at 4). However, the Examiner relies on Heijningen as allegedly teaching these features of claim 1.

Heijningen relates to a method for determining noise generated from mixed-signal ICs, and alleges to overcome problems with conventional noise analyses which factor only certain aspects that contribute to noise generation. For example, by forming digital circuitry and analog circuitry on the same substrate, the digital circuitry injects noise on the substrate that affects analog circuitry. (See Heijningen, ¶ 0009). Analysis of such noise generation is said to be very complex, and typically involves assumptions which in turn lessen accuracy of the analysis. (See Heijningen, ¶ 0010). It is alleged further that gate dependency cannot be accurately modeled and substrate noise from a power supply is not taken into account. (See Heijningen, ¶ 0012-13).

Heijningen alleges to overcome these issues with basically a two-part simulation. The first simulation includes "a one-time characterization of all digital standard cells to extract substrate current generation for every possible switching combination ...." (Heijningen, ¶ 0099, lines 2-5). In fact, this "standard cell characterization is performed once for every technology." (Heijningen, ¶ 0103, lines 7-8). Macro models created include detailed substrate models for each standard cell and generated switching noise and power waveforms for all possible combinations. These models are compiled into a single library in advance, e.g., by using a circuit simulator such as SPICE. (See Heijningen, ¶ 0100, lines 1-8).

The second simulation is a "gate level simulation, e.g. a VHDL gate level simulation (with an extracted VHDL gate library), for each design to extract the switching events." (Heijningen, ¶ 0099, lines 4-7). All switching events are recorded and collected in a switching file. (See Heijningen, ¶ 0101, lines 3-4). In other words, using a simulator, Heijningen alleges to obtain records of switching events of the gate and to calculate the waveform of the noise current. (See Heijningen, ¶ 0127).

A macro model selected from the library created during the first simulations is combined with the switching event data for the second simulation. This combination is alleged to result in an equivalent substrate model for the entire digital circuit and is used to simulate the total generated noise. (See Heijningen, ¶ 0102).

A. The Office Action Fails To Identify Any Teaching Of A Time-Division Group Of Parasitic Capacitors

The Office Action posits that Heijningen teaches the "time-division" features of claim 1. The Office Action states: "determining the power supply noise requires determining a capacitance contribution for each cell (i.e. capacitor group) independently (i.e. time division groups) (0119) and combining the individual waveforms to determine the total noise waveform (0127)." (Final Action at 9). Appellant disagrees.

The description referenced by the Office Action concerns determining power supply noise induced in a substrate during the first simulation for generating macro models, as described above. Paragraph 119 has been reproduced below.

> To accurately simulate noise coupling from the power supply, the ringing effects should also be included in the macro model. This requires that the circuit capacitance Ccir between power and ground is extracted for each cell and added to the macro model. This extraction is performed by a small signal (AC) simulation of the digital gate without the substrate model.

It appears that the Office Action relies on the statement "circuit capacitance Ccir between power and ground is extracted for each cell and added to the macro model." Importantly, a cell represents a group of gates, which may include substrate resistors and well capacitors. (See Heijningen, ¶ 0078, lines 6-8, and ¶ 0088, lines 1-5). Heijningen charges a cell (including a group of capacitors), and records the results in the macro model library, and then re-configures the cell (including a group of capacitors) for a different switching combination (it represents the digital circuit differently), charges, and records the results of that cell to the macro model library. (Heijningen, ¶ 0099, lines 2-5). This way, different switching combinations of the digital circuit may be compiled in a single library. Still, any given representation of a digital circuit taken from this library does not correspond to a "time-division group of parasitic capacitors."

An overly broad interpretation of "time-division" pervades the above reasoning. A requirement for "Independent" evaluation of each capacitor group (i.e. cell) configuration does not read on the "time-division group of parasitic capacitors," contrary to the assertion in the Office Action. Claim 1 recites representing a digital circuit...as a time-division group of parasitic capacitors and generating an analyses model by coupling the time-division group of parasitic capacitors. An exemplary manner in which the time-division group is represented and connected is seen in Figs. 1-2 of the present application. Heijningen, on the other hand, merely provides that there are multiple configurations of the cell (including a group of capacitors) evaluated. Yet, there is no disclosure or suggestion of the

manner in which the group of parasitic capacitors are represented and connected – whether it is in "time-division," as claim 1 requires. The unique "time-division" feature is not taught nor suggested by Heijningen. It is possible that Heijningen defines connections of the capacitor group in accordance with the truth table of Nagata. Whether each configuration is evaluated independently is irrelevant.

B. The Office Action Fails To Identify Any Teaching Of "Determining The Waveform Of The Source Current In The Digital Circuit From The Analysis Model," As Claim 1 Recites

For reasons not completely understood, referring to paragraph 0127, the Examiner alleges that Heijningen discloses or suggests "determining the waveform of the source current in the digital circuit from the analysis model," as claim 1 recites. (See Final Action at 4). Here, Heijningen merely states that total noise is determined by accumulating all individual waveforms belonging to the switching events. Heijningen does not teach the claimed analysis model, which as claimed is generated by connecting the "time-division group of parasitic capacitors." It follows that Heijningen does not teach "determining the waveform of the source current in the digital circuit from the analysis model," as claim 1 recites.

C. The Office Action Has Not Provided A Legally Cognizable Or Logical Motivation For The Substitution And Modification Urged In The Final Rejection

It is submitted that the allegation in support of motivation in the rejection is basically flawed. The paragraph spanning pages 4 and 5 of the Final Action has been reproduced below in parts.

> It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata to include determining the waveform of the source current in the digital circuit from the analysis mode and specifying that the parasitic capacitors be a time-series group of parasitic capacitors, as taught by Heijningen...

Appellant disagrees. As stated above, there is no disclosure or suggestion representing a digital circuit with, and generating an analysis further to connections of, a time-division group of parasitic

capacitors, and determining the waveform of the source current from the analysis model. The Office Action continues:

> ... because Nagata does teach determining the noise as represented by voltage waveforms as well as that the capacitor groups are charged at specific timing according to the output of a truth table and, as suggested by Heijningen the combination would have provided a method for correctly determining the effect of capacitances (0088, lines 18-28), a simplified substrate and gate model based substrate voltage profile using a current profile (0089, lines 7-21), and a corresponding method for obtaining the power supply waveform by determining the effect of each group individually and then combining the waveforms of each group (0119 and 0127) in order to quickly and accurately determine the noise in a system having a large amount of gates ...

Appellant disagrees.

It is the Examiner's burden to establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, the [Examiner] must, *inter alia*, show 'some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teaches of the references.' *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d1596, 1598 (Fed. Cir. 1988). 'The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one or ordinary skill in the art, or, on some cases the nature of the problem to be solved.' *Kotzab*, 217 F.3d at 1370, 55 USPQ2d at 1317."" *In re Thrift*, 298 F.3d 1357 (Fed. Cir. 2002).

Heijningen determines capacitances for multiple switching configurations of a digital circuit, but does not disclose the particular switching configurations. Nagata discloses representing a digital circuit as a group of capacitors, switched in accordance with an input selected from a truth table. Neither disclose the deficiencies discussed above.

Here, the Examiner has clearly not met its burden. The Examiner's assertions of motivation correspond to very generalized statements in Heijningen concerning the advantages of the two part simulation for determining substrate noise characteristics. Specifically, the purported motivation – for

"a method for correctly determining the effect of capacitances (0088, lines 18-28), a simplified substrate and gate model based substrate voltage profile using a current profile (0089, lines 7-21), and a corresponding method for obtaining the power supply waveform by determining the effect of each group individually and then combining the waveforms of each group (0119 and 0127)" – is directed to Heijningen's method of simulating numerous switching configurations, and storing the results of these configurations for application to actual circuit simulations. Yet, the Examiner has not established how one of ordinary skill in the art would have been led to combine the references to arrive at that claimed. The fact that Heijningen discloses determining capacitances for multiple switching configurations of a digital circuit does not as a matter of fact make the combination obvious (especially considering there is basically no relationship between determining capacitances for numerous switching combinations and representing, and generating an analysis model of, a digital circuit as a time-division group of parasitic capacitors, as claim 1 recites).

Of course, any asserted motivation must be "clear and particular, and it must be supported by actual evidence." (emphasis added) *Teleflex, Inc. v. Ficosa North American Corp.*, 299 F.3d 1313, 1334 (Fed. Cir. 2002). The allegations made by the Examiner, with respect to quickly and accurately determining the noise in a system having a large amount of gates, is not evidence that is clear and particular. *In re Lee,* 277 F.3d 1338 (Fed Cir. 2002) ("When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation or suggestion to select and combine the references relied on as evidence of obviousness." (emphasis supplied)). Here, the Examiner has simply restated the claim limitations not found in the prior art, paraphrased Heijningen directed to a different simulation method that has nothing to do with that claimed, with the factually unsupported and improperly conclusory preamble "[i]t would have been obvious ..." This is precisely the reversible error discussed in *Lee.*

* * * *

For the above reasons, the Examiner has failed to establish a *prima facie* case of obviousness. The Board is respectfully requested to reverse this rejection.

II. Rejection of Claim 7 under 35 U.S.C. §103(a) – Nagata in view of Heijningen and Mitra

As claim 7 includes all the limitations set forth in claim 6, which in turn includes the limitations recited by claim 1, claim 7 is not obvious for the reasons discussed above. The Board is respectfully requested to reverse this rejection.

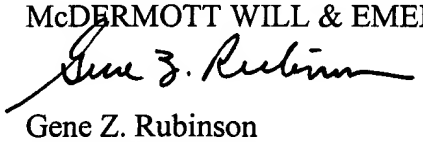
Moreover, Mitra fails to cure the deficiencies in the other applied references discussed above. Mitra proposes isolating analog circuitry from digital circuitry using a substrate-noise evaluation mechanism to determine optimal layout for reducing noise. The evaluation mechanism utilizes a set of placement algorithms. However, Mitra fails to disclose or suggest the "time-division" limitations of claim 1. Hence, it fails to cure the deficiencies discussed above.

Conclusion

Based upon the arguments submitted supra, Appellant respectfully submit that the Examiner's rejections under 35 U.S.C. § 103 are not legally viable. Appellant, therefore, respectfully solicits the Honorable Board to reverse the Examiner's rejections and find the grounds of rejection of the claims on appeal to be in error.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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Please recognize our Customer No. 20277 as our correspondence address.

CLAIMS APPENDIX

1. A method of analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, comprising:

representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit, as a time-division group of parasitic capacitors comprising parasitic capacitors each connected between a source line and a ground line to be charged at a specific timing, and a group of parasitic capacitors each charged statically;

generating an analysis model by coupling one end of the time-division group of parasitic capacitors, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line; and

determining the waveform of the source current in the digital circuit from the analysis model.

2. The method according to claim 1, wherein the digital circuit is divided into a plurality of segments along a border at which the parasitic impedances of the source line and the ground line are locally increased, the time-division group of parasitic capacitors and the group of the parasitic capacitors statically charged are assigned for a group of the logic gates included in each segment.

3. The method according to claim 1, wherein each parasitic capacitor included in the time-division group of parasitic capacitors is determined every predetermined time interval, and wherein a length of the time interval is set according to a frequency of the switching operations of the logic gates in a period of time at which the parasitic capacitors are determined.

4. The method according to claim 3, wherein the length of the time interval is set to be of shorter as the frequency of the switching operations is greater.

5. The method according to claim 1, wherein a capacitance of the parasitic capacitor to be charged at a specific timing is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed.

6. A method of analyzing a substrate noise comprising:

regarding, as a substrate noise, a change in voltage which is caused by an interaction between the source current in the digital circuit determined from the analysis model and the parasitic impedances of the source line and the ground line; and

using the method of claim 1 with the regarded change in voltage to analyze the substrate noise.

7. A method of designing a semiconductor integrated circuit which includes analog and digital circuits, comprising:

receiving a design specification;

designing the analog and digital circuits according to the design specification;

analyzing a substrate noise generated in the digital circuits using the method of claim 6; and

re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing a result of the substrate noise analysis so that a design specification is satisfied.

8. An apparatus for analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, comprising:

arrangement for representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit, as a time-division group of parasitic capacitors comprising parasitic capacitors each connected between a source line and a ground line to be charged at a specific timing, and a group of parasitic capacitors each charged statically;

arrangement for generating an analysis model by coupling one end of the time-division group of parasitic capacitors, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line; and

arrangement for determining the waveform of the source current in the digital circuit from the analysis model.

9. The apparatus according to claim 8, wherein the digital circuit is divided into a plurality of segments along a border at which the parasitic impedances of the source line and the ground line are locally increased, the time-division group of parasitic capacitors and the group of the parasitic capacitors charged statically are assigned for a group of the logic gates included in each segment

10. The apparatus according to claim 8, wherein each parasitic capacitor included in the time-division group of parasitic capacitors is determined every predetermined time interval, and wherein a length of the time interval is set according to a frequency of the switching operations of the logic gates in a period of time at which the parasitic capacitors are determined.

11. The apparatus according to claim 10, wherein the length of the time interval is set to be of shorter as the frequency of the switching operations is greater.

12. The apparatus according to claim 8, wherein a capacitance of the parasitic capacitor to be charged at a specific timing is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed.

13. The method according to claim 1, wherein each capacitor of the time-division group of parasitic capacitors is charged at different times in accordance with a predetermined time interval.

14. The apparatus according to claim 8, wherein each capacitor of the time-division group of parasitic capacitors is charged at different times in accordance with a predetermined time interval.